An Approach to Practical Validation of Control Software Specification

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- 1. Automotive control software development
- 2. Specification validation and open issues
- 3. Concept of the practical approach
- 4. Tool implementation
- 5. Application
- 6. Summary and future direction

Definition of Verification and Validation

Standard definitions

Verification

- Confirmation by examination and provision of objective evidence that specified requirements and are fulfilled
- Ensuring implementation satisfies the requirements for that step. Can include testing, analysis and review
- You built product right

Validation

- Confirmation by examination and provision of objective evidence that particular requirements for a specific intended use are fulfilled
- Ensuring requirements are complete and correct
- You built the right product



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Automotive control system and software

Major automotive control systems



- Interacting with physical environment and various drivers
- Growing contribution of elaborate control systems to deliver attractive products and to meet regulations

Coping with growing complexity is a big challenge

Traditional Development Process



Example : Developing Cold Start Control of Gasoline Engine

Target

Reduce 5% Hydro Carbon emission

Concept

Activate catalyst converter as fast as possible

Control design

Optimize reference profiles of throttle, fuel injection and spark timing.



Supposed prototyping loops



System engineering is exploration of feasible solution



- Due to growing complexity, hard to foresee exploration paths without prototyping
- Solution space is getting narrower

Improvement of prototyping loops is the key

Model-Based Development



Model-based Development of Control Software



Areas where further improvement is needed

- Validation of code specification
- Lack of documents/evidence



Summary - Automotive control software development



 Requires repetitive prototyping loops for feasible solution exploration



 Promotion of Model-based Development to improve prototyping loop efficiency



• Specification validation is a big challenge

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Validation of code specification



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Making development process formal and accountable



No need to care about samples! – exhaustiveness assured

Formal process and verification - lessons learned



- Property must be simply describable relative to the Design

So far applicable area is limited.





Waterfall Formal Large system Scalable Modular Accountable Team/Rule oriented Redundant



In Japan:

- Low communication cost
- Cultural strength

- ...

On the way to finding the best level of formality

A practical problem - latent function

Under a rare condition, hunting behavior had occurred. The cause was an unrecognized dependence loop.



Due to complex dependence among function, especially via shared memory, one function was overlooked and the condition hadn't been exercised due to its rareness.

C code is to blame for ... ?

Another practical problem - latent function in a Simulink model

It seems there is no latency in models, but it is not as obvious as we suppose.



Redundant paths in a Simulink model authored by system engineer

Supposed reasons of incomprehensibility:

- Lack of software design skill or less care about model quality
- Essential paths are obscured by software level design details (e.g. type guard)
- Functional grouping is not an easy task

Summary - Specification validation and open issue



•"Is the sample set enough?"



- Current usage of formal verification is limited
- On the way to finding the best level of formality



• One of validation problem: Latent function

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A direction to go - whitebox

Testing with software coverage metrics

Make sure branches and conditions of each switch are exercised





Requires case-by-case inference of validity at system level (or use close-loop simulator)

Problems:

- Are functional components really covered?
- Bad S/N for functional coverage (importance of branches are not even)
- Hard to infer validity without knowing which function was stimulated



There is a chance of div by 0 error with 100% branch coverage

Hard to get a sense of functional coverage

Functional coverage



Coverage is supposed to be sufficient if each of equivalence class of function is exercised in proper manner respectively.



Specification validation by design interest extraction

Defect category and our target



Our target : Are functional components covered?

Expected benefits of the approach

- Interactive process with visual support stimulates engineer's awareness
- Mechanized interest extraction serves as the baseline of coverage standard
- Quality of validation can be improved by tuning extraction mechanism



Summary - Concept of the practical approach



•Our target is latency problem



• Covering equivalence class of function



- Extract design interest : equivalence class of function and their behaviors
- Visual support enhances engineers' awareness

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Outline of current tool implementation



DFG with edge selection condition





Points unique to embedded control software



Example

```
int _sc_, gvar1, gvar2, gvar3;
int * const gvar_tbl[3] = {&gvar1, &gvar2, &gvar3};
void timed_task(void){
 foo();
                                                                                 2
                                                                      =
 bar();
 baz();
}
                                                        =
                                                                  gvar1
                                                                                            3
                                                                                 =
void foo(void){
 gvar1 = 1;
void bar(void)
                                                                              gvar2
                                                                                            =
 int i, P, sum;
 sum = 0;
                                                                                         gvar3
 for (i = 0; i < 3; i++) {
                                          Reference to previously
  sum += *(gvar_tbl[i]);
                                          executed value
 }
 _sc_ = sum;
                                                Order is undecidable
void baz(void){
 gvar2 = 2;
                                                                                      =
void occasional_event(void){
                                                                                     SC
 gvar3 = 3;
```

Model abstraction

Replace typical function patterns to compact representation:

- to omit trivial branches
- to help comprehension
 - Type guard
 - Absolute
 - Rounding
 - Max/Min
 - Summation
 - Cast
 - ...



On Control flow graph



Snapshot DFG as a decomposed functional component

Enumerate possible dataflow patterns by taking edge combinations



Meaning of the snapshot breakdown

Original C code



Slicing criteria

Narrowing focus of interest with visual comprehension

Behavioral analysis for extracted snapshot



Instrument C code and find inputs which passes the target path.





*1 "CIL: Intermediate Language and Tools for Analysis and Transformation of C Programs" by George C. Necula, Scott McPeak, S.P. Rahul and Westley Weimer, in "Proceedings of Conference on Compilier Construction", 2002.

*2 http://www.cprover.org/cbmc/

Example

Input: gin1, gin2 Output: _sc_

1:	<pre>int gin1, gin2, _sc_ ;</pre>				
2:	void foo (void)				
4:	{				
5: 6:	int P, Q, R, x, y, out ;				
7: 8:	P = (gin1 == 10); Q = (gin1 * gin2 > 0); P = ((gin1 + gin2 < 0));				
9. 10:	$\mathbf{R} = \left(\left(\operatorname{gini} + \operatorname{gini} < 0 \right) \otimes \left(\operatorname{gini} > 5 \right) \right)$				
11: 12:	if (P) { x = 1;				
13:	} else {				
14:	x = 2i				
15:	}				
16:	if (Q) {				
17:	y = 3;				
18:	} else {				
19:	y = 4i				
20:					
21:					
22:	out = x;				
23:	} else {				
24:	out = y;				
25:	}				
26:					
27: 28:	<pre>sc = out;</pre>				



Statistics:

ALL	267
OK	21
NG	246
Coverage	7.86516853933%

Test generation result: No test input activating 655 767 819 843 853 864 **OK** #1 1 snap#2 was found 772 819 843 853 864 655 674 690 710 753 767 NG #2_1 43 853 864 655 NG #3_1 F 843 853 864 655 674 NG #4 1 819 843 853 655 674 13 NG #5 1 Step-by-step identification of root conflict by solving relaxed constraints 819 843 853 655 674 713 716 #6_1 NG F Т 843 853 864 655 674 710 753 767 2 819 NG #7 1 F 843 853 864 655 674 753 767 819 **OK** #8 1 F 655 674 843 853 864 690 710 713 819 753 767 **OK** #9 1 F F

Example of the root conflict

Statistics:

ALL	267
OK	21
NG	246
Coverage	7.86516853933%

Test generation result:

ок	#1_1	655 767 819 843 853 864 T F T F T F
Conflict	#2_1	674 772 F F
Conflict	#3_1	674 772 F F
Conflict	#4_1	674 772 F F
Conflict	#5_1	674 772 F F
Conflict	#6_1	674 772 F F
Conflict	#7_1	710 772 F F
ок	#8_1	655 674 677 690 710 713 72 T T F F T F T
ок	#9_1	655 674 677 690 710 713 72 T T F F T F F
Conflict Conflict Conflict OK OK	#4_1 #5_1 #6_1 #7_1 #8_1 #9_1	F F 674 772 F F 674 772 F F 710 772 F F 655 674 677 690 710 713 72 T T F F T F T 655 674 677 690 710 713 72 T T F F T F T 655 674 677 690 710 713 72 T T F F T F F 7 T F F T F F



Existence of conflict is fine. Unrecognized conflict is the problem.



 Dataflow graph and its snapshots as one of the model of functional component



• Auto test generators for behavioral analysis



- Model checking based one shot test generator
- Tests pinpointing the particular snapshot
- Conflict analysis

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Monitoring snapshot coverage on SILS



SILS simulation

Paths reduction in a production code



Architecture analysis of large scale legacy code



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Future direction

Tool implementation

- DFG extraction from Simulink model
- Integration to SILS/HILS environment

Abstraction level of equivalence class of function

- Extract more essential function for larger problems
- Other function models

Auto test generators

Software modeling



Auto test generators





Software modeling

Demand for software modeling:

- Embeddable (can generate C code)
- Helps intuitive understanding of equivalence class of function
- Separation of concern
 - Implementation details Essential function
- Unique (no manual synchronization among models)

Centralized mode control





- + Clear mode of operation
- Redundant description

Distributed mode control



- + Compact description
- Ambiguous mode of operation

Is it possible to describe as a static model??

End.